AMENDMENTS TO THE CLAIMS

1. (Canceled)
2. (Canceled)
3. (Canceled)
4. (Canceled)
5. (Canceled)
6. (Canceled)
7. (Canceled)
8. (Canceled)
9. (Cancelled)
10. (Cancelled)
11. (Cancelled)
12. (Cancelled)
13. (Cancelled)

14. (Currently Amended) A data storage circuit comprising:

a comparison section for reading out existing data stored in a storage element to compare said existing data and new data with each other prior to writing of said new data to said storage element, wherein:

when the comparison section determines that the existing data and the new data are identical, the new data is not written to the storage element, and

when the comparison section determines that the existing data and the new data are not identical, the new data is written to the storage element; and

a control signal generating section for generating a readout control signal and a write control signal from a write signal input to said control signal generating section, said readout control signal for performing readout control of the existing data and ~~a~~ said write control signal for performing write control of the new data, wherein

the existing data and the new data are compared with each other in the comparison section in accordance with the write control signal from the control signal generating section;

wherein said control signal generating section includes an AND logic gate for generating said readout control signal, and a NOR logic gate for generating said write control signal; and

wherein the pulse of the readout control signal and write control signal are shorter than the pulse of the write signal input to said control signal generating section.

15. (Currently Amended) A method for writing data in a data storage circuit, comprising:

reading out existing data stored in a storage element prior to writing new data to the storage element to compare the existing data and the new data to each other;

writing the new data to the storage element when the existing data and said new data are identical with each other, and so as to perform the write process of said new data to said storage element in a case where said existing data and said new data are not identical with each other; and

generating a readout control signal and a write control signal in accordance with a write signal input to the data storage circuit;

reading out the existing data in accordance with the readout control signal; and

comparing the existing data with the new data in accordance with the write control signal;

wherein said generating step includes using an AND logic gate to generate said readout control signal, and a NOR logic gate to generate said write control signal; and

wherein the pulse of the generated readout control signal and write control signal are shorter than the pulse of the write signal input to the data storage circuit.

16. (Currently Amended) A data storage device comprising:

a comparison section for reading out existing data stored in a storage element and compare the existing data and new data to each other prior to writing the new data to the storage element, wherein

when the comparison section determines that the existing data and new data are identical, the new data is not written to the storage element, and

when the comparison section determines that the existing data and new data are not identical, the new data is written to the storage element;

a control signal generating section for generating a readout control signal and a write control signal from a write signal input to said control signal generating section, said readout control signal for performing readout control of the existing data and a write control signal for performing write control of the new data, wherein the existing data and the new data are compared to each other in the comparison section, in accordance with a control signal from said control signal generating section;

wherein said control signal generating section includes an AND logic gate for generating said readout control signal, and a NOR logic gate for generating said write control signal; and

wherein the pulse of the readout control signal and write control signal are shorter than the pulse of the write signal input to said control signal generating section.

17. (Previously Presented) The data storage device as described in claim 16, wherein the comparison section comprises:

a new data retention section for temporarily retaining the new data;

an existing data retention section for temporarily retaining the existing data; and

a write enable signal generating section for comparing the new data retained in the new data retention section and the existing data retained in the existing data retention section with each other to control an output of the write enable signal,

wherein,

the new data is temporarily retained in the new data retention section while the existing data is temporarily retained in the existing data retention section in response to the readout control signal output from the control signal generating section, and

the new data retained in the new data retention section and the existing data retained in the existing data retention section are compared to each other in response to the write control signal output from the control signal generating section.

18. (Cancelled)

19. (Cancelled)

20. (Previously Presented) The data storage device according to claim 17, wherein said new data retention section and existing data retention section include input control transistors for controlling the retaining of the new data and the existing data in accordance with readout control signal.

21. (Previously Presented) The data storage device according to claim 17, wherein the write enable signal generation section includes output control transistors for controlling comparison of the new data and the existing data in accordance with the write control signal.

22. (Previously Presented) The data storage device according to claim 17, wherein the write enable signal generation section includes an XOR logic gate for generating a write enable signal in accordance with the new data and the existing data.